What is claimed is:

1. A local area network, comprising:

a) a data bus having a multiple of eight parallel data lines;

b) a clock bus;

c) a plurality of bus ports coupled to said data bus and said clock bus, each bus port including a transceiver coupled to each of said data lines, an input buffer coupled to said transceivers, an output buffer coupled to said transceivers, and a hardware interface coupled to said buffers, wherein at least two bus ports have different hardware interfaces.

2. A local area network according to claim 1, further comprising a power bus, each of said bus ports being coupled to said power bus and drawing power therefrom.

3. A local area network according to claim 1, wherein said hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire(TM) port link.

4. A local area network according to claim 1, wherein said input and output buffers are each two kilobyte FIFOs.

5. A local area network according to claim 1, wherein data is transferred on the data bus in a repeating, variable length frame.

6. A local area network according to claim 5, wherein said frame is defined by a plurality of clock cycles, at least one of which is reserved for bidding for access to transmit on the data bus.

7. A local area network according to claim 6, wherein each of said ports has a unique address defining a unique priority value.

8. A local area network according to claim 7, wherein following the bidding cycle, access to the bus is granted to the port having the highest priority and the other bidding port addresses are placed in a queue in order of priority.

9. A local area network according to claim 8, wherein each port maintains a copy of the queue.

10. A local area network according to claim 7, wherein following the bidding cycle, at least one cycle is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus.

11. A parallel bus local area network, including a plurality of ports with each port having a unique address assigned thereto defining a unique priority value, comprising:

a) means for generating a repeating, variable length frame;

b) port control means for bidding for access to the bus during at least one predefined clock cycle of the frame; and

c) a bus controller for granting access to the bidding port having the highest priority and placing the other bidding port addresses in a queue.

12. Apparatus according to claim 11 wherein each port maintains a copy of the queue.

13. Apparatus according to claim 11 wherein bidding is only permitted when the queue is empty.

14. Apparatus according to claim 11 wherein at least one cycle of the frame is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus.

15. Apparatus according to claim 14 further comprising:

d) means for enabling the port having access to the data bus to transmit a message length during the message length cycle of the frame; and

e) means for enabling the port having access to the data bus to transmit a destination address during the destination address cycle of the frame.

16. Apparatus according to claim 15, further comprising:

f) means for enabling the port having the destination address to assert the busy signal during the busy cycle of the frame; and

g) means for enabling the port attempting to transmit to the busy port to repeat bidding until the message is sent.

17. A local area network, comprising:

a) a data bus having a plurality of parallel data lines; and

b) a clock bus having a clock frequency, wherein said local area network has a bandwidth equal to the product of the number of said plurality of data lines times said clock frequency, and said bandwidth is scalable by increasing the number of said plurality of data lines and/or increasing said clock frequency.

18. A local area network according to claim 17, further comprising a plurality of bus ports coupled to said data bus and said clock bus, wherein each of said bus ports has an address defined by a data line and a clock cycle.

19. A local area network, comprising:

a) a data bus having a plurality of parallel data lines; and

b) a clock bus having a clock frequency; and

c) a plurality of bus ports coupled to said data bus and said clock bus, wherein each of said bus ports has a configurable hardware interface.

20. A local area network according to claim 19, wherein said configurable hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire (TM) port link.

21. A local area network, comprising:

a) a parallel data bus;

b) a clock bus; and

c) a plurality of bus ports coupled to said data bus and said clock bus, wherein said local area network becomes more efficient as usage increases.

22. A local area network, comprising:

a) a parallel data bus;

b) a clock bus;

c) a plurality of bus ports coupled to said data bus and said clock bus; and

d) collision avoidance means for completely avoiding data collisions.

23. A local area network according to claim 22, wherein said means for completely avoiding data collisions includes arbitration means whereby only one bus port is permitted to transmit at one time.

24. A local area network, comprising:

a) a parallel data bus;

b) a clock bus;

c) a plurality of bus ports coupled to said data bus and said clock bus;

d) arbitration means whereby bus ports bid for access to the data bus; and

e) glare avoidance means whereby two simultaneous bids are resolved.

25. A local area network according to claim 24, wherein said glare avoidance means includes means for determining priority of bus ports and assigning access to the data bus to the highest priority bus port when simultaneous bids occur.